

M5M5256AP, AFP-70, -85, -10, -70L, -85L, -10L

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

MITSUBISHI (MEMORY/ASIC)

DESCRIPTION

This M5M5256AP, AFP is a 262,144-bit CMOS static RAM organized as 32,768-words by 8-bits which is fabricated using high-performance double polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM. It is ideal for the memory systems which require simple interface.

The stand-by current is low enough for a battery back-up application. It is mounted in a standard 28 pin package and configured in an industrial standard 32K x 8-bit pinout.

FEATURES

Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5256AP, AFP-70 M5M5256AP, AFP-85 M5M5256AP, AFP-10	70n 85ns 100ns	70mA	2mA
M5M5256AP, AFP-70L M5M5256AP, AFP-85L M5M5256AP, AFP-10L	70ns 85ns 100ns		100μA

- Single +5V Power Supply
- No Clocks, No Refresh
- Data-Hold on +2V Power Supply
- Directly TTL Compatible: All Inputs and Outputs
- Three-State Outputs: OR-tie Capability
- Simple Memory Expansion by $\bar{S}$
- $\bar{OE}$ Prevents Data Contention in the I/O Bus
- Common Data I/O
- Package

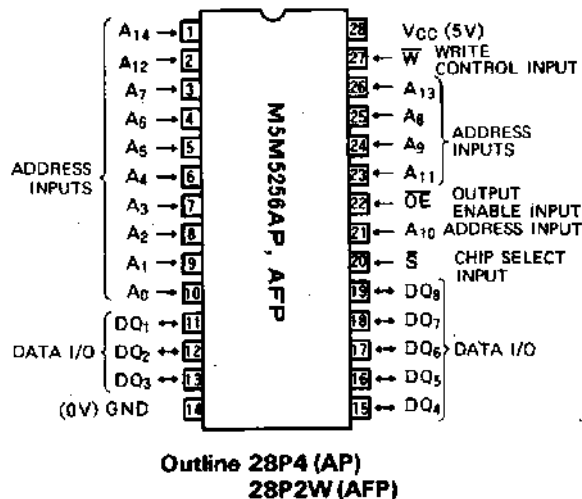
M5M5256AP 28 Pin 600mil DIP

M5M5256AFP . . 28 Pin Small Outline Package (SOP)

APPLICATION

Small Capacity Memory Units.

PIN CONFIGURATION (TOP VIEW)

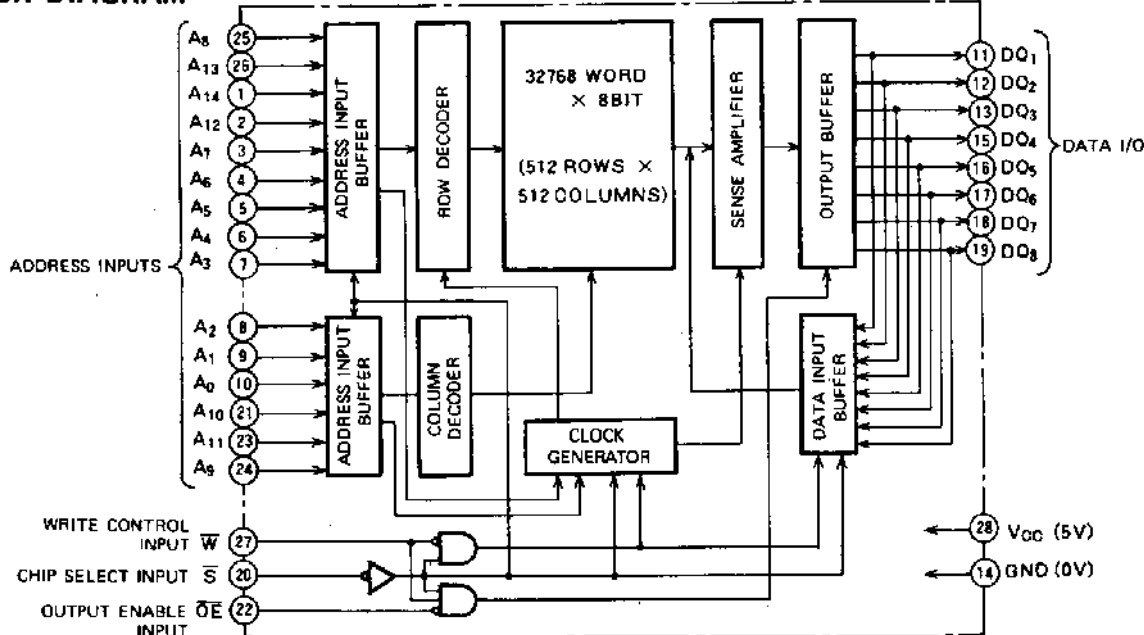


FUNCTION

The operation mode of the M5M5256AP, AFP is determined by a combination of the device control inputs $\bar{S}$, $\bar{W}$ and $\bar{OE}$. Each mode is summarized in the function table. (see next page)

A write cycle is executed whenever the low level $\bar{W}$ overlaps with the low level $\bar{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\bar{W}$, $\bar{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\bar{OE}$ directly controls the output stage. Setting the $\bar{OE}$ at a high level, the output stage is in a high-impedance

BLOCK DIAGRAM



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state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state.

When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4} , and the memory data can be held +2V power supply, en-

abling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	I_{CC}
H	X	X	Non selection	High-impedance	Standby
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	Active
L	H	H		High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	-0.3 ~ 7	V
V_I	Input voltage		-0.3 ~ $V_{CC} + 0.3$	V
V_O	Output voltage		0 ~ V_{CC}	V
P_d	Power dissipation	$T_a = 25^\circ\text{C}$	700	mW
T_{opr}	Operating temperature		0 ~ 70	$^\circ\text{C}$
T_{stg}	Storage temperature		-65 ~ 150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ($T_a = 0 \sim 70^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
V_{IL}	low input voltage	-0.3		0.8	V
V_{IH}	high input voltage	2.2		$V_{CC} + 0.3$	V

ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High input voltage		2.2		$V_{CC} + 0.3$	V
V_{IL}	Low input voltage		-0.3		0.8	V
V_{OH}	High output voltage	$I_{OH} = -1\text{mA}$	2.4			V
V_{OL}	Low output voltage	$I_{OL} = 2\text{mA}$			0.4	V
I_I	Input current	$V_I = 0 \sim V_{CC}$			± 1	μA
I_O	Output current	$\overline{S} = V_{IH}$ or $\overline{OE} = V_{IH}$, $V_{I/O} = 0 \sim V_{CC}$			± 1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\overline{S} < 0.2$, $\overline{W} > V_{CC} - 0.2$, Output open Other input < 0.2 or $> V_{CC} - 0.3$ Min. cycle		30	65	mA
I_{CC2}	Active supply current (AC, TTL level)	$\overline{S} = V_{IL}$, $\overline{W} = V_{IH}$, Output open Other input $= V_{IL}$ or V_{IH} Min. cycle		35	70	mA
I_{CC3}	Stand by supply current	$\overline{S} \geq V_{CC} - 0.2\text{V}$ Other inputs $= 0 \sim V_{CC}$	AP, AFP		2	mA
					100	μA
I_{CC4}	Stand by supply current	$\overline{S} = V_{IH}$, Other inputs $= 0 \sim V_{CC}$			3	mA
C_i	Input capacitance ($T_a = 25^\circ\text{C}$)	$V_I = \text{GND}$, $V_i = 25\text{mVrms}$, $f = 1\text{MHz}$			6	pF
C_o	Output capacitance ($T_a = 25^\circ\text{C}$)	$V_O = \text{GND}$, $V_O = 25\text{mVrms}$, $f = 1\text{MHz}$			8	pF

Note 1. Direction for current flowing into IC is indicated as positive (no mark).

2. Typical value is $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$.

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262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM**SWITCHING CHARACTERISTICS** ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise noted)**Read cycle**

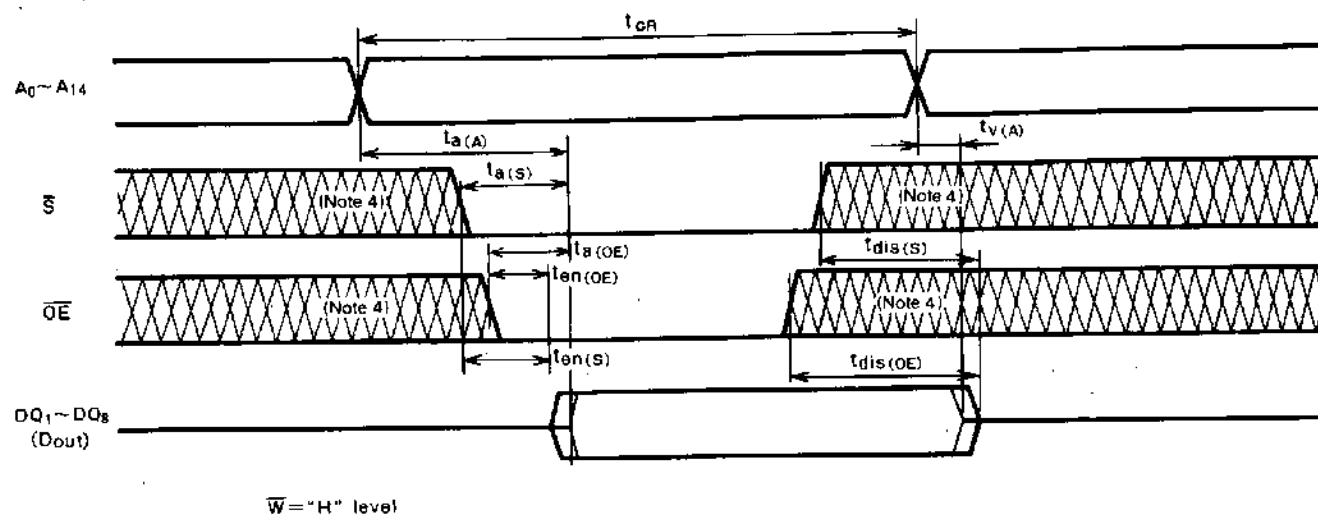
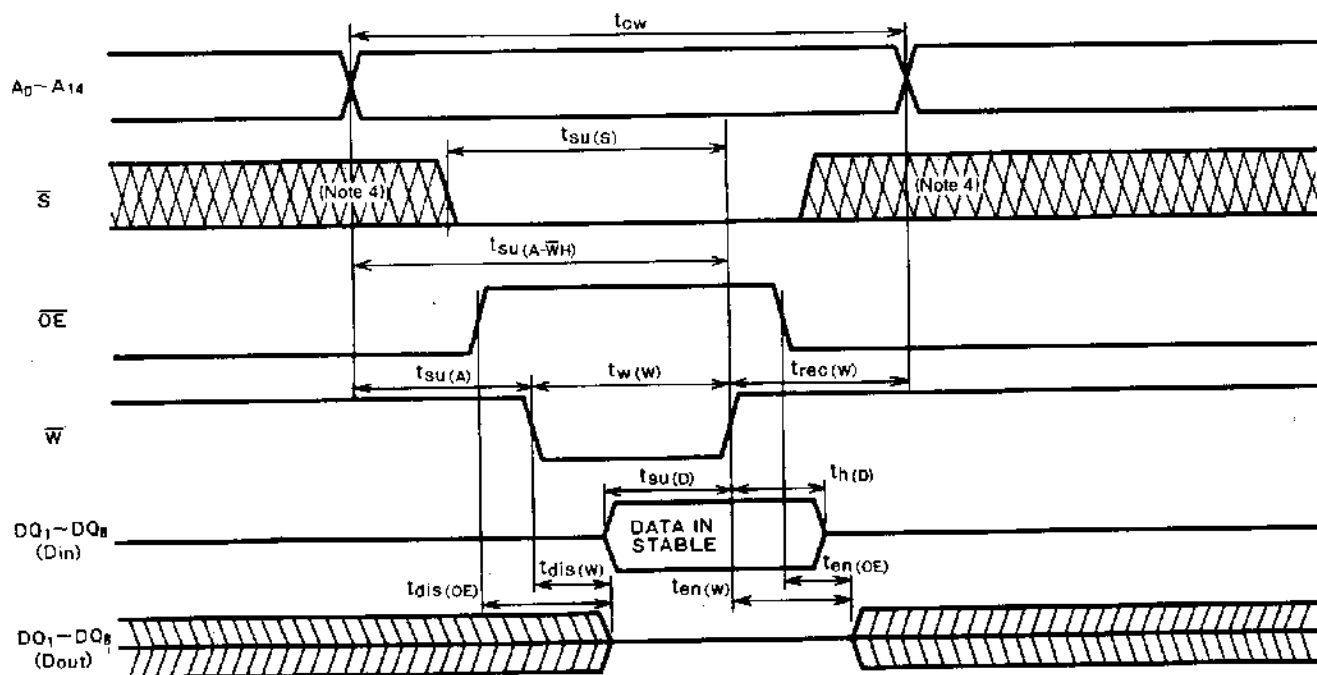
Symbol	Parameter	Limits									Unit
		M5M5256-70 M5M5256-70L			M5M5256-85 M5M5256-85L			M5M5256-10 M5M5256-10L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t _{CR}	Read cycle time	70			85			100			ns
t _a (A)	Address access time			70			85			100	ns
t _a (S)	Chip select access time			70			85			100	ns
t _a (OE)	Output enable access time			35			45			50	ns
t _{dis} (S)	Output disable time after $\overline{S}$ high			30			30			35	ns
t _{dis} (OE)	Output disable time after $\overline{OE}$ high			30			30			35	ns
t _{en} (S)	Output enable time after $\overline{S}$ low	5			5			10			ns
t _{en} (OE)	Output enable time after $\overline{OE}$ low	5			5			10			ns
t _v (A)	Data valid time after address change	20			20			20			ns

TIMING REQUIREMENTS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise noted)**Write cycle**

Symbol	Parameter	Limits									Unit
		M5M5256-70 M5M5256-70L			M5M5256-85 M5M5256-85L			M5M5256-10 M5M5256-10L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	70			85			100			ns
$t_{W(W)}$	Write pulse width	55			60			60			ns
$t_{su}(A)$	Address set up time	0			0			0			ns
$t_{su}(A-\overline{W}H)$	Address set up time with respect to $\overline{W}$ high	65			75			80			ns
$t_{su}(S)$	Chip select set up time	65			75			80			ns
$t_{su}(D)$	Data set up time	30			35			35			ns
$t_h(D)$	Data hold time	0			0			0			ns
$t_{rec}(W)$	Write recovery time	0			0			0			ns
$t_{dis}(W)$	Output disable time after $\overline{W}$ low			25			30			35	ns
$t_{dis}(OE)$	Output disable time after $\overline{OE}$ high			25			30			35	ns
$t_{en}(W)$	Output enable time after $\overline{W}$ high	5			5			10			ns
$t_{en}(OE)$	Output enable time after $\overline{OE}$ low	5			5			10			ns

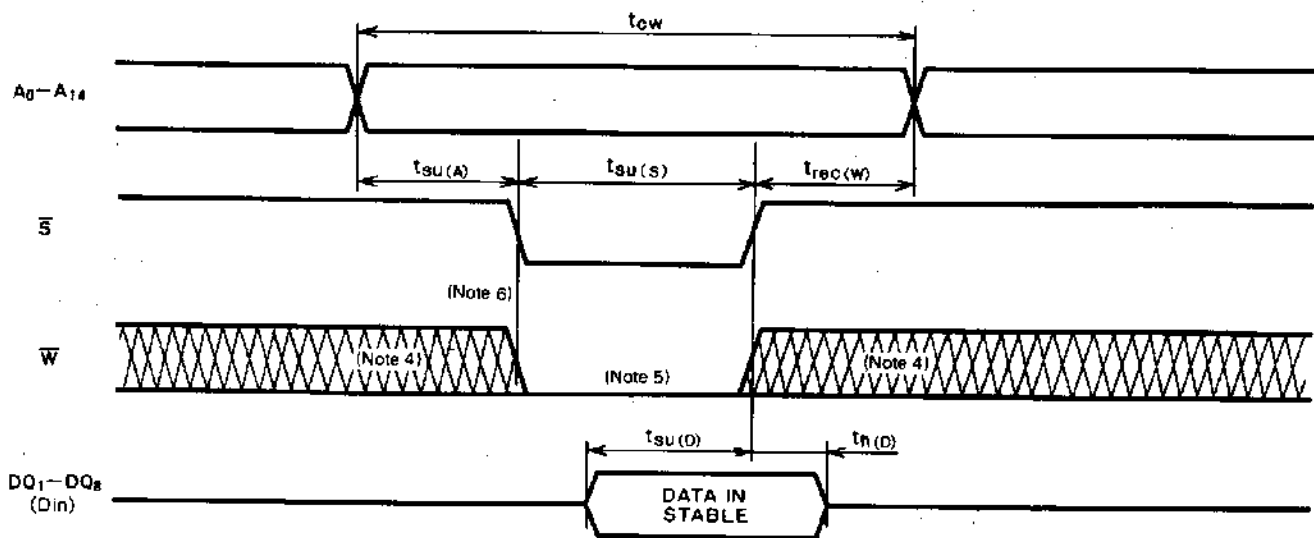
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262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM**TIMING DIAGRAM****Read cycle****Write cycle ($\overline{W}$ control)**

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Note 3: Test condition

Input pulse level: 0.6 ~ 2.4V

Input pulse rise, fall time, 10ns

Load: 1 TTL. $C_L = 30\text{pF}$ for -70, -70L, 100pF for -85, -10, -85L, -10L.

Conditions of assessment: 1.5V

4: Hatching indicates the state is don't care.

5: Writing is executed in overlap of $\bar{S}$ and $\bar{W}$ low.6: If $\bar{W}$ goes low simultaneously with or prior to $\bar{S}$, the output remains in the high-impedance state.

7: Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS**ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, unless otherwise noted)**

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage		2			V
$V_I(\bar{S})$	Chip select input $\bar{S}$	$2.2\text{V} \leq V_{CC(PD)}$	2.2			V
		$2\text{V} \leq V_{CC(PD)} \leq 2.2\text{V}$		$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	$V_{CC}=3\text{V}$, Other inputs = 3V			2	mA
		AP, AFP			50	
		AP, AFP-L				μA

TIMING REQUIREMENTS ($T_a = 0 \sim 70^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{SU(PD)}$	Power down setup time		0			ns
$t_{REC(PD)}$	Power down recovery time		t_{CR}			ns

POWER DOWN CHARACTERISTICS