OKI semiconductor

MSM16811

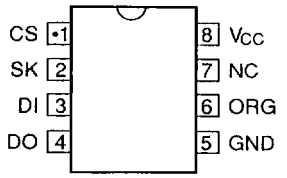
1,024-BIT SERIAL E²PROM

FEATURES

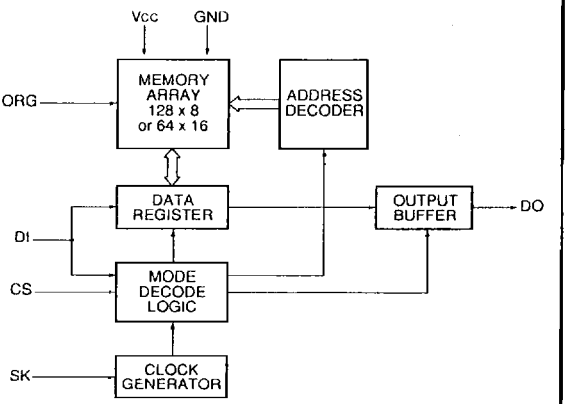
- CMOS Floating Gate Technology
- Single +5-volt supply
- Eight pin plastic package
- 64 x 16 or 128 x 8 user selectable serial memory
- Compatible with NS9346
- Self timed programming cycle with Auto-Erase
- Word and chip erasable
- Operating range 0°C to 70°C
- 10,000 erase/write cycles
- 10 year data retention

PIN CONFIGURATION (TOP VIEW)

8 Pin Dual-In-Line
8 Pin S.O. Package



FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTIONS			
CS	Chip Select	ORG	Memory Array Organization Selection Input. When the ORG pin is connected to +5 V the 64 x 16 organization is selected. When it is connected to ground the 128 x 8 organization is selected. If the ORG pin is left unconnected, an internal pull-up device selects the 64 x 16 organization.
SK	Clock Input		
DI	Serial Data Input		
DO	Serial Data Output		
V_{CC}	+5 V Power Supply		
NC	No Connection		
GND	Ground		

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INSTRUCTION SET							
Instruction	Start Bit	Opcode	Address		Data		Comments
			128 x 8	64 x16	128 x 8	64 x16	
READ	1	1 0	$A_6 - A_0$	$A_5 - A_0$			READ Address $A_N - A_0$
ERASE	1	1 1	$A_6 - A_0$	$A_5 - A_0$			ERASE Address $A_N - A_0$
WRITE	1	0 1	$A_6 - A_0$	$A_5 - A_0$	$D_7 - D_0$	$D_{15} - D_0$	WRITE Address $A_N - A_0$
EWEN	1	0 0	11XXXXX	11XXXX			Program Enable
EWDS	1	0 0	00XXXXX	00XXXX			Program Disable
ERAL	1	0 0	10XXXXX	10XXXX			Erase All Addresses
WRAL	1	0 0	01XXXXX	01XXXX	$D_7 - D_0$	$D_{15} - D_0$	Program All Addresses

Power-On Data Protection Circuitry: During power-up all modes of operation are inhibited until Vcc has reached a level of approximately 3.0 volts. During power-down the source data protection circuitry inhibits all modes when Vcc falls below the voltage range of approximately 3.0 volts.

ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATING

Rating	Symbol	Conditions	Value	Unit
Supply Voltage	V_{CC}	Ta = 25°C	−0.3 ~ 7	V
Input Voltage	V_I		−0.3 ~ V_{CC} + 0.3	V
Output Voltage	V_O		−0.3 ~ V_{CC} + 0.3	V
Storage Temperature	T_{STG}		−55 ~ + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Conditions	Range	Unit
Supply Voltage	V_{CC}	–	5 ± 10%	V
Temperature Range	Ta	–	0 ~ 70	°C
Data Hold Temperature	Ta	–	0 ~ 70	°C

DC CHARACTERISTICS

(Vcc = 4.5V to 5.5V, Ta = 0°C ~ 70°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Value		Unit	Notes
			Min	Max		
Supply Voltage	V_{CC}	–	4.5	5.5	V	
Power Supply Current	I_{CC1}	V_{CC} = 5.0 V CS = 1	–	3	mA	
	I_{CC2}	V_{CC} = 5.5 V CS, KS, DI = 0V DO, ORG = OPEN	–	100	µA	
"L" Input Voltage	V_{IL}	–	–0.1	0.8	V	
"H" Input Voltage	V_{IH}	–	2.0	V_{CC}+1	V	
"L" Output Voltage	V_{OL}	TTL I_{OL} = 2.1 mA	–	0.4	V	
		CMOS I_{OL} = 100 µA	–	0.1	V	
"H" Output Voltage	V_{OH}	TTL I_{OH} = -400 µA	2.4	–	V	
		CMOS I_{OH} = -100 µA	V_{CC}-0.5	–	V	
Input Leakage Current	I_{LI}	V_{in} = 5.5 V	–	10	µA	
Output Leakage Current	I_{LO}	V_{out} = 5.5 V CS = 0	–	10	µA	

AC CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Unit	Notes
			Min	Typ	Max		
CS Setup Time	t_{CSS}	–	0.2	–	–	µs	
CS Hold Time	t_{CSH}	–	0	–	–	µs	
DI Setup Time	t_{DIS}	–	0.4	–	–	µs	
DI Hold Time	t_{DIH}	–	0.4	–	–	µs	
Output Delay to 1	t_{PD1}	CL = 100pF	–	–	2	µs	
Output Delay to 0	t_{PD0}	V_{OL} = 0.8, V_{OH} = 2.0	–	–	2	µs	
Output Delay to HiZ	t_{HZ}	V_{IL} = 0.45V, V_{IH} = 2.4	–	–	0.4	µs	
Erase/Write Pulse Width	t_{EW}	–	–	–	10	ms	
Min CS Low Time	t_{CSMIM}	–	1	–	–	µs	
Min SK High Time	t_{SKHI}	–	1	–	–	µs	
Min SK Low Time	t_{SKLOW}	–	1	–	–	µs	
Output Delay to Status Valid	t_{SV}	CL = 100pF	–	–	1	µs	
Maximum Frequency	SK_{MAX}	–	0	–	250	kHz	

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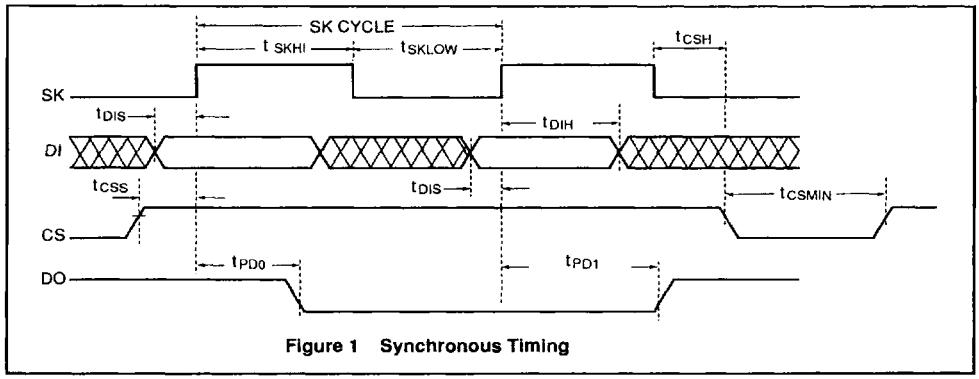


Figure 1 Synchronous Timing

Device Operation

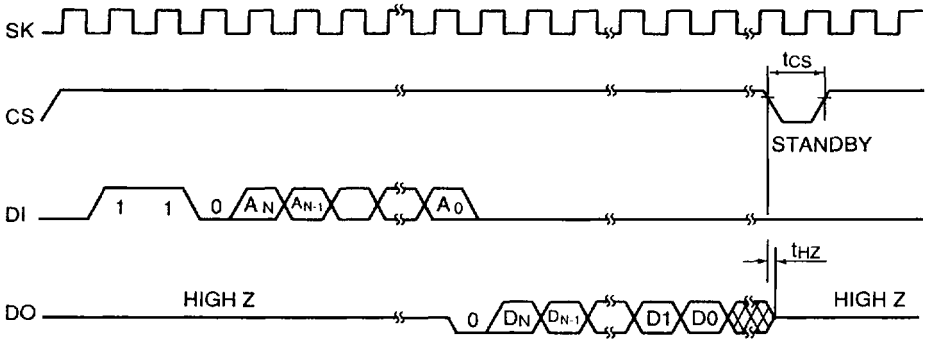
The MSM16811 has 7 instructions that allow it to read, erase, or write. Each instruction consists of a start bit logical 1, an opcode field (2 bits or 4 bits) and an address field (6 or 7 bits).

The DO pin is a multiplexed pin. It is used as Data Out during the Read mode. It can also be used as a Ready Busy status indicator in programming mode. In all the other modes DO is tri-stated.

During power-up all modes of operation are disabled and the device comes up in a program disabled state. An EWEN instruction must be issued before starting to program.

At power-down, when Vcc falls below a level of approximately 3V, the data protection circuitry inhibits all modes of operation and an EWDS instruction is executed internally.

READ



Organization	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

The READ instruction reads the contents of the addressed register. It outputs data serially on the DO pin. After the instruction is decoded, a dummy bit (logical 0) precedes the output data string.

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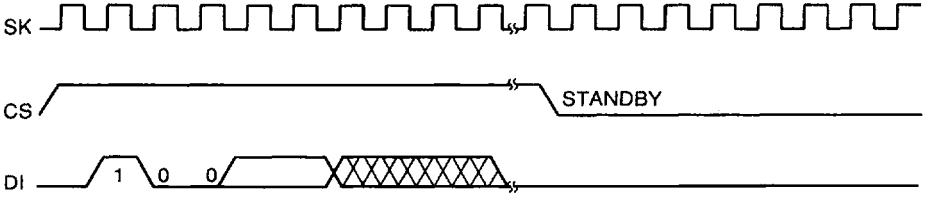
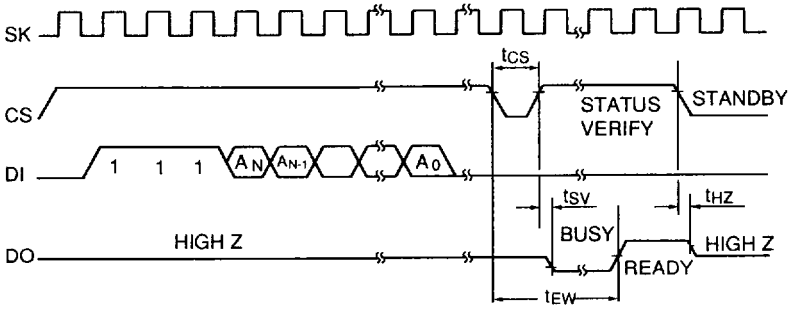
EWEN/EWDS (ERASE/WRITE ENABLE AND DISABLE)



ENABLE = 11 64 x 16 = 4 X's
DISABLE = 00 128 x 8 = 5 X's

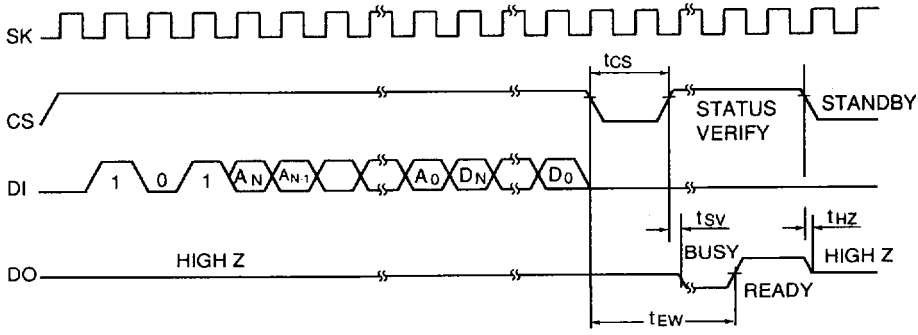
After power-up and before starting any programming instruction the EWEN instruction must be issued. Once it is issued, it remains active until an EWDS instruction takes place. The EWDS instruction prevents any accidental programming of the part. The READ instruction is independent from the EWEN and EWDS instructions.

ERASE



After an ERASE instruction is shifted in, CS is dropped low. This sets the beginning of the self timed erase sequence. If CS is then brought high (after observing the tcs spec) the DO pin will act as a status indicator. It will remain low so long as the chip is programming. It will go high after all the the bits of the addressed register are set to a logical 1.

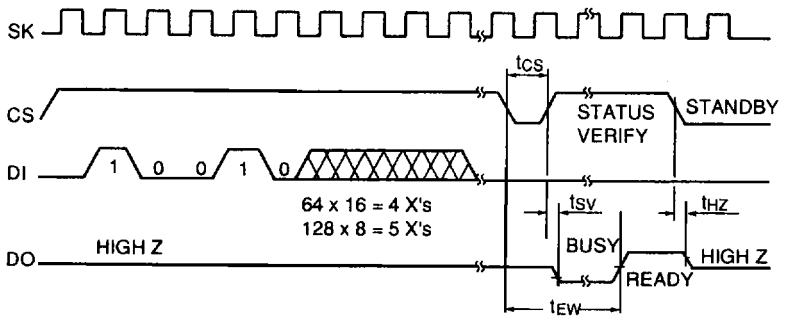
WRITE



After a WRITE instruction is shifted in with the corresponding 8 bits or 16 bits of data, CS is dropped low. This sets the beginning of the self timed programming sequence. If CS is brought high during the programming time (after observing the tcs specification), the DO pin will act as a status indicator – it will remain low so long as the chip is programming. It will go high after all the bits of the addressed register are set to their proper values. With the MSM16811 it is NOT neccessary to erase the memory location before the WRITE instruction.

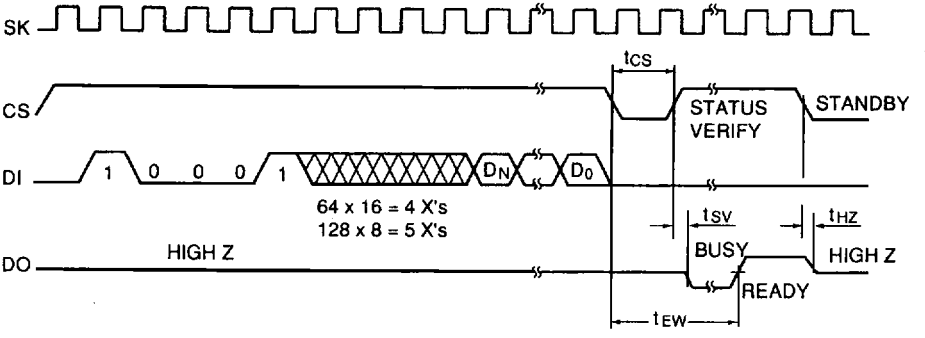
Configuration	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

ERAL (ERASE ALL)



The ERAL instruction erases the whole chip. Except for its different opcode, the ERAL instruction is identical to the ERASE instruction.

WRAL (WRITE ALL)



The WRAL instruction writes to all the registers simultaneously. All the registers must be erased before a WRAL operation. Except for its different opcode, the WRAL instruction is identical to the WRITE instruction.

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