Advance Information

Triple 8-Bit Video DAC

CMOS

MC44200

FU SUFFIX
QFP PACKAGE
CASE 824A–01

ORDERING INFORMATION
MC44200FU 44 Pin QFP

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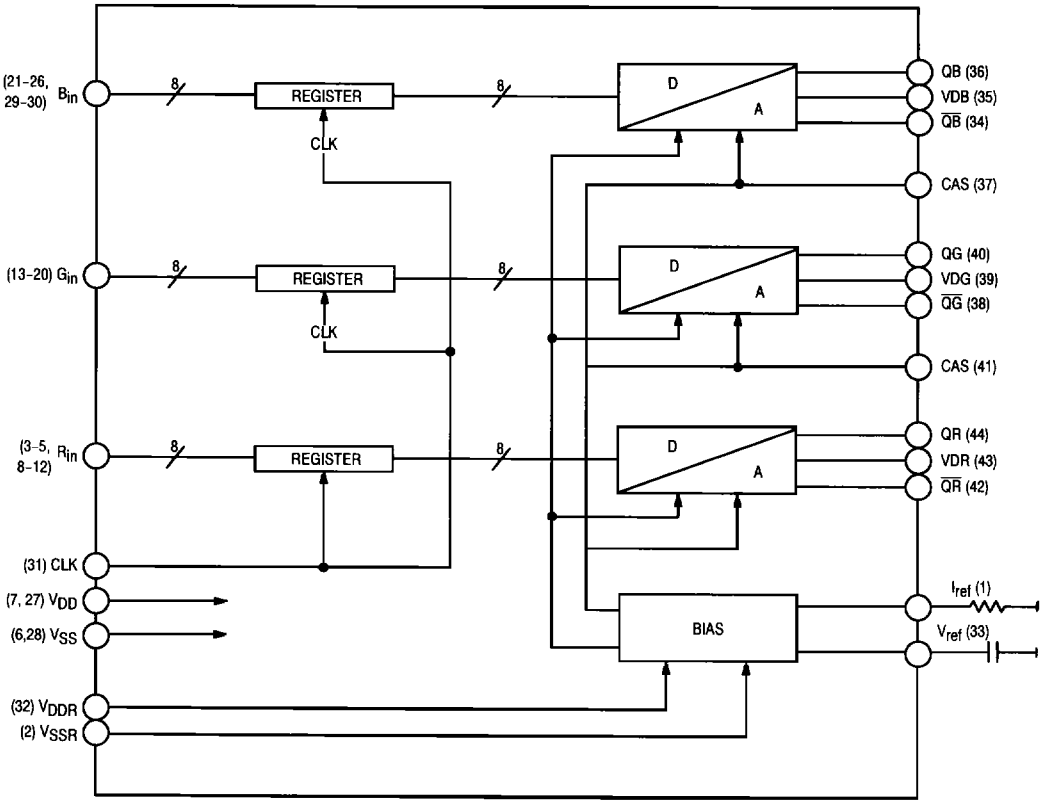
The MC44200 contains three independent Digital to Analog Converters (DAC). The digital to analog conversion is accomplished by means of a bank of binary controlled differential current sources.

Furthermore, differential outputs are provided. The MC44200 is especially suitable as a converter in TV–picture digital processing (e.g. picture–in–picture) and Compact Disk–Interactive (CD–i) applications.

- 55 MHz Max Conversion Speed
- Differential Outputs
- Adjustable Output Current Range
- TTL Compatible Inputs
- Integrated Reference Voltage
- Single 5 V Power Supply

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (T_A = + 25°C unless otherwise specified)

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Rating	Value	Unit
T_{stg}	Storage Temperature	– 65 to +150	°C
T_A	Operating Ambient Temperature	– 40 to + 85	°C
I_{in}	Maximum Current Per Input Pin	± 10	mA
I_{out}	Maximum Current Per Output Pin	± 50	mA
	Maximum Current V_{ref} Pin	± 10	mA
V_{in}, V_{out}	Maximum Voltage All Pins	– 0.5 to V_{DD} + 0.5	V
P_D	Power Dissipation	700	mW
V_{DD}	DC Supply Voltage	– 0.5 to + 6	V

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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ELECTRICAL CHARACTERISTICS (T_A = – 40 to + 85°C unless otherwise specified; V_{DD} = 5.0 V ± 5%)

Symbol	Characteristic	Min	Max	Unit	Note
V_{DD}	Power Supply Voltage	4.5	5.5	V	
$I_{DD(D)}$	Digital Supply Current		20	mA	
$I_{DD(R)}$	Reference Supply Current		15	mA	
$I_{DD(AH)}$	DAC High Current Mode Supply		30	mA	
$I_{DD(AL)}$	DAC Low Current Mode Supply		15	mA	
C_{out}	Output Capacitance		10	pF	
K	Internal Current Gain	5.1	5.5		
DAC High Current Mode (Note 1)					
V_{out}	Maximum Output Voltage	0	V_{DD} – 2.1	V	
I_{out}	Full scale Output Current	16	22	mA	
DNL	Differential Non Linearity		0.5	LSB	
INL	Integral Non Linearity		1	LSB	
ΔI_{out}	DAC to DAC Max Output Current Matching		2	%	
t_{tr}	Transition Time		8	ns	2
t_{settle}	Settling Time 50% to 98% of Step		30	ns	2
t_d	Analog Output Delay Time		50	ns	2
Δt_d	Output Delay Time Difference Between Channels		2	ns	
P_{SS}	Power Supply Sensitivity @ V_{out} (Full Scale = 1 V)		0.25	%	5
DAC Low Current Mode (Note 3)					
V_{out}	Output Voltage Range	0	V_{DD} – 1.5	V	
I_{out}	Full Scale Output Current	8	11	mA	
DNL	Differential Non Linearity		0.5	LSB	
INL	Integral Non Linearity		1	LSB	
ΔI_{out}	DAC to DAC Output Current Matching		2	%	
t_{tr}	Transition Time		15	ns	4
t_{settle}	Setting Time 50% to 98% of Step		110	ns	4
t_d	Analog Output Delay Time		70	ns	4

ELECTRICAL CHARACTERISTICS (T_A = – 40 to + 85°C unless otherwise specified; V_{DD} = 5.0 V ± 5%)
DAC Low Current Mode (continued)

Symbol	Characteristic	Min	Max	Unit	Note
Δt_d	Output Delay Time Difference Between Channels		4	ns	
P_{SS}	Power Supply Sensitivity @ V_{out} (Full Scale = 3 V)		1.2	%	5

NOTES:
1. R_I_{ref} = 330 Ω, no external resistive load or voltage applied to pin 33.
2. Load R_L = 37.5 Ω , C_L = 15 pF.
3. R_I_{ref} = 660 Ω, no external resistive load or voltage applied to pin 33.
4. Load R_L = 300 Ω, C_L = 5 pF.
5. The change of the output voltage with change in the power supply voltage. This parameter is expressed in % change of full scale output versus % change of V_{DD}.

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DATA INPUTS

Symbol	Characteristic	Min	Max	Unit
V_{IH}	Input High Level	2		V
V_{IL}	Input Low Level		1.2	V
t_{su}	Data Setup Time	4		ns
t_h	Data Hold Time	1		ns
C_{in}	Input Capacitance		7	pF

CLOCK INPUT

Symbol	Characteristic	Min	Max	Unit
V_{IH}	Input High Level	2		V
V_{IL}	Input Low Level		0.8	V
V_{hys}	Hysteresis	0.3		V
t_{cl}	Clock Low Duration	5		ns
t_{ch}	Clock High Duration	5		ns
t_r	Clock Rise Time		15	ns
t_f	Clock Fall Time		15	ns

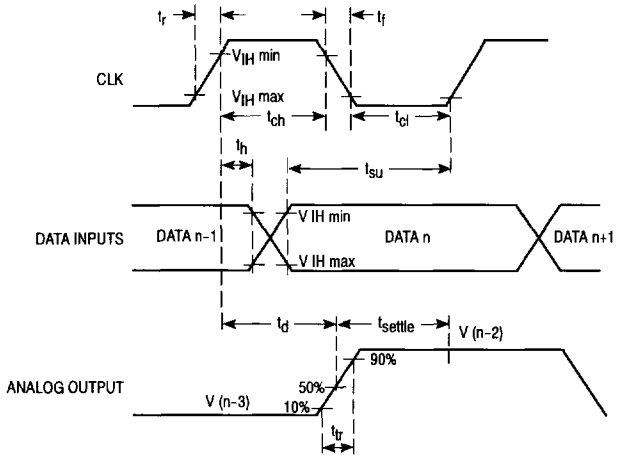

Figure 1. Clock Input and Output Timing

VOLTAGE REFERENCE

Symbol	Characteristic	Min	Max	Unit
V_{ref}	Reference Voltage	1.173	1.297	V
V_{ref} Ext	External Reference Voltage (Note 1)	1.111	1.359	V
ZV_{ref}	Output Impedance (Note 2)	10	50	kΩ

NOTES:
1. $V_{DD(R)}$ must be connected to + 5 V.
2. Load placed on external reference voltage by internal V_{ref} circuitry.

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PIN ASSIGNMENTS

Pin No.	Name	Function
1	I_{ref}	To external R_I_{ref}
2	$V_{SS(R)}$	V_{SS}, reference
3	R7	Input, red, bit 7
4	R6	Input, red, bit 6
5	R5	Input, red, bit 5
6	V_{SS}	V_{SS}, digital
7	V_{DD}	V_{DD}, digital
8	R4	Input, red, bit 4
9	R3	Input, red, bit 3
10	R2	Input, red, bit 2
11	R1	Input, red, bit 1
12	R0	Input, red, bit 0
13	G7	Input, green, bit 7
14	G6	Input, green, bit 6
15	G5	Input, green, bit 5
16	G4	Input, green, bit 4
17	G3	Input, green, bit 3
18	G2	Input, green, bit 2
19	G1	Input, green, bit 1
20	G0	Input, green, bit 0
21	B7	Input, blue, bit 7
22	B6	Input, blue, bit 6

Pin No.	Name	Function
23	B5	Input, blue, bit 5
24	B4	Input, blue, bit 4
25	B3	Input, blue, bit 3
26	B2	Input, blue, bit 2
27	V_{DD}	V_{DD}, Digital
28	V_{SS}	V_{SS}, Digital
29	B1	Input, blue, bit 1
30	B0	Input, blue, bit 0
31	CLK	Clock input
32	$V_{DD(R)}$	V_{DD}, Reference
33	V_{ref}	Reference voltage, (I/O)
34	QB	Output blue (inverted)
35	VDBL	V_{DD} of blue DAC
36	QB	Output blue (true)
37	CAS	Cascade bias, to ext. C
38	QG	Output green (inverted)
39	VDGR	V_{DD} of green DAC
40	QG	Output green (true)
41	CAS	Cascade bias, to ext. C
42	QR	Output red (inverted)
43	VDRD	V_{DD} or red DAC
44	QR	Output red (true)

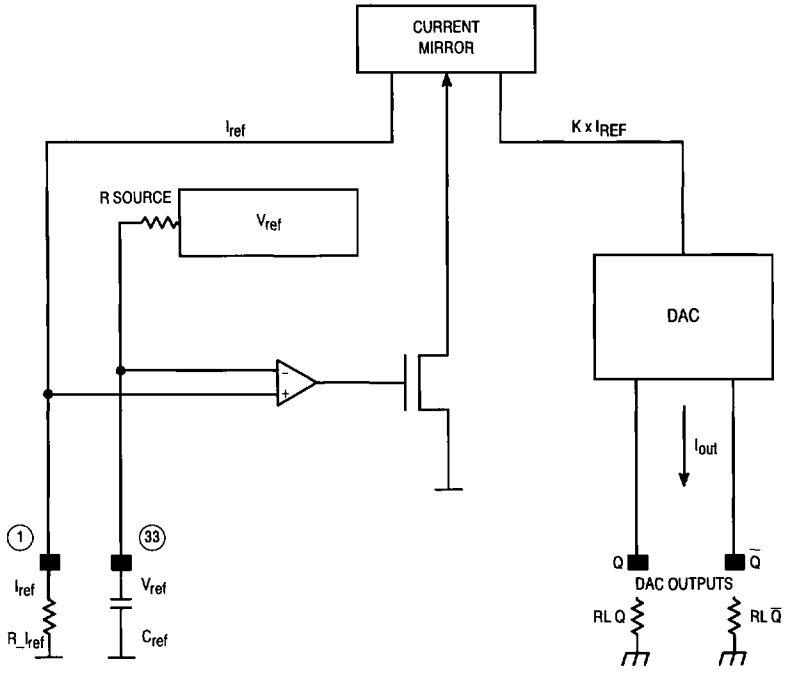
GENERAL DESCRIPTION

The MC44200 contains three parallel 8–bit digital to analog converters with common clock with a Schmitt trigger input and an internal reference supply. Each 8–bit word input to the device is stored in an internal register on the rising edge of the clock signal and is converted to an analog value by a bank of binary controlled differential current sources. The output current is determined by an integrated band–gap reference circuit, and an external resistor connected to I_{ref} (see Figure 2).

The MC44200 may be forced to operate from an external reference by connecting the external reference voltage to terminal V_{ref} (pin 33). This voltage should be within the range 1.235 V ± 10%. The internal circuitry loading on the external voltage source will be between 10 KΩ to 50 KΩ. Calculation of output drive is accomplished in the same manner as when using an internal source.

Each digital to analog converter supplies its output in the form of a differential current source. The two outputs allow the device to drive either a differential balanced line, one single unbalanced line or two complementary unbalanced lines. The outputs can drive up to 20 mA each providing 0.75 V drive into a doubly terminated 75 Ω line or 1.5 V into a single terminated line.

The output current is presetable using the external resistor (R_{ref}) at the maximum conversion rate for output current between the range of: 8 mA < I_{out} < 22 mA. *See Current Modes (High and Low).* The device can be operated at reduced output current however conversion rate and settling time must correspondingly be derated.



NOTE: $I_{out} = (V_{ref}/R_{ref}) \times K$
$V_{out} = I_{out} \times R_{LOAD}$ (Q or $\overline{Q}$)

Figure 2. MC44200 Current Bias Network

PIN DESCRIPTIONS

SUPPLY PINS

$V_{DD(D)}$ (Pins 7, 27)
VDRD (Pin 43), VDGR (Pin 39), VDBL (Pin 35)
$V_{DD(A)}$ for Red, Green and Blue Outputs
$V_{DD(R)}$ (Pin 32)

The three types of supply pins are digital, analog and reference. The dc voltage applied to all four pins must be maintained such that

$$V_{DD(D)} = V_{DD(A)} = V_{DD(R)}.$$

Each pin must be carefully decoupled to ground as close to the package as possible and particular care should be taken with $V_{DD(R)}$ as any noise present on this pin will appear in the output data as an equivalent input noise. This noise will be present on the RD, GR and BL output pins in a ratio of 1:1 to the input noise (worse case condition). Noise reduction can be improved by incorporating choke coil inductors in series with the power supply rails.

GROUND PINS

V_{SS} (Pins 6, 28) Digital Ground
$V_{SS(R)}$ (Pin 2) Reference Supply Ground

Since the analog output is a differential drive current source, no analog ground pin is needed. By returning the unused output to ground, an analog reference is established for the active output.

ANALOG OUTPUTS

QR (Pin 44)
$\overline{QR}$ (Pin 42)
QG (Pin 40)
$\overline{QG}$ (Pin 38)
QB (Pin 36)
$\overline{QB}$ (Pin 34)

The converted analog signals are output at these pins. QR, QG and QB are the true output pins while $\overline{QR}$, $\overline{QG}$ and $\overline{QB}$ provide the complementary inverted outputs. These outputs are configured as differential current drivers with a maximum current drive for each output of 20 mA. Voltage drive is determined by the value of the resistance used to program the I_{ref} pin and the value of the load on the output pins. For example, the voltage delivered to a 150 Ω load for an output programmed for 10 mA would be:

$$V_{out} = i * RL = 10\ mA * 150 = 1.5\ V.$$

When driving an unbalanced line, the unused outputs should be returned to analog ground through a resistance equal to the load on the active output pins.

OTHER ANALOG PINS

CAS (Pins 37, 41)

These pins are used for external decoupling of the internal reference circuitry for the D/As. Typically a 10 nF capacitor is connected between pin 37 and analog V_{DD}, a 470 nF capacitor is connected between pin 41 and analog V_{DD}, and pins 37 and 41 are connected together (see Figure 8).

I_{ref} (Pin 1)

This pin is used to program the value of the load current delivered by the Red, Green and Blue output pins. The value of the resistance connected between this pin and reference ground is found by the formula:

$$R_{ref} = (1.235\ V/I_{out}) \times 5.3$$

for typical values for the internal circuitry.

DIGITAL INPUTS

R0 – R7 (Pins 12 – 8, 5, 4, 3)
G0 – G7 (Pins 20 – 13)
B0 – B7 (Pins 30, 29, 26 – 21)

These pins are the parallel inputs of the digital value for the RGB signals. R0 through R7 is the digital value of the RED component, G0 through G7 is the digital value of the GREEN and B0 through B7 is digital value of the BLUE component.

CLK (Pin 31)

The rising edge of the signal supplied to this pin is used to latch the input signals into the internal registers. These registers hold the digital RGB component data for conversion by the triple D/A converters.

DIFFERENTIAL OUTPUTS

Each digital to analog converter supplies a differential output current pair whose relationship is shown in Figure 3. These outputs function in push–pull, or complementary, fashion to provide drive to a differential balanced line. The outputs may also be used to drive an unbalanced line with either in phase operation or complementary (180 degree) inversion.

When only one output is used to supply a single unbalanced current, the load on the digital to analog converter output should be balanced by placing a load on the unused output equal in value to the load on the unused output. This can be a single resistor whose value is equal to the load impedance.

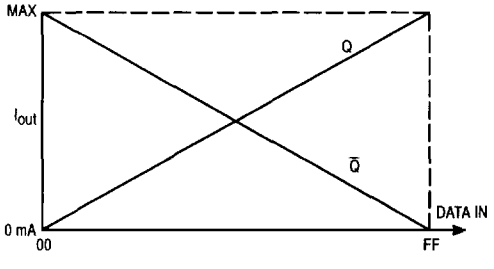


Figure 3. Q versus $\overline{Q}$

CURRENT MODES (HIGH AND LOW)

The full scale output current is determined by the external resistor R_{ref}. The high current mode (R_I_{ref} = 330 Ω) is intended to be used when the analog outputs are connected directly with a monitor going through a coaxial cable. The low current mode (R_I_{ref} = 660 Ω) may be used when the outputs are going to buffers. The full scale output current varies linearly with the external resistor R_I_{ref}.

V_{out}

The output voltage supplied to the load is determined by the value of the load impedance and the value chosen for

the external bias resistor R_{ref}. The high current mode (R_{ref} = 330 Ω) is usually intended to drive a monitor directly through a coaxial cable. When external buffering is supplied, the low current (R_{ref} = 660 Ω) mode may be used. The full scale current varies linearly with the value of R_{ref} over the range of 330 Ω to 660 Ω without derating. The reference current generated in R_{ref} by the reference voltage V_{ref} is multiplied by the current gain of the conversion circuitry. This current gain is the factor K and has a typical value of 5.3. I_{out} can be calculated using the formula:

$$I_{out} = (V_{ref}/R_{ref}) \times K.$$

For a typical value for V_{ref} of 1.235 V, a typical value for K of 5.3 and a peak current value of 13 mA, the value for R_{ref} should be 510 Ω.

$$R_{ref} = (1.235\ V/13\ mA) \times 5.3 = 504\ \Omega, \text{ use } 510\ \Omega.$$

The output voltage, V_{out}, is a product of the output drive and the load impedance (Norton's Theorem).

$$V_{out} = I_{out} \times R_{LOAD} \text{ (Q or } \overline{Q}).$$

Figures 4 and 5 show two different load implementations for the same line impedance.

In Figure 4, the 75 Ω transmission line is terminated both at the load and at the source. The effective load on the output of the MC44200 for this doubly terminated 75 Ω line is one half the line impedance or 37.5 Ω. The peak output voltage for this arrangement is limited to 0.75 V.

$$V_{out} = I_{out} \times R_{LOAD} = 20\ mA \times 37.5 = 0.75\ V.$$

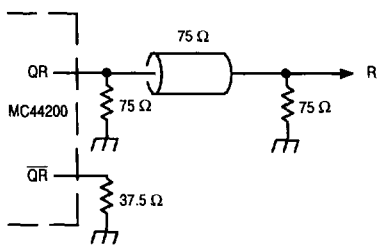
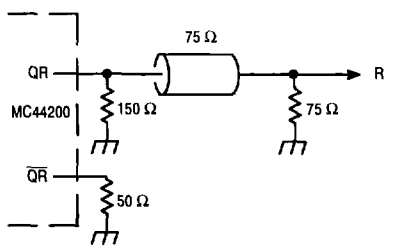


Figure 4. Resistive Load for V_{out} = 750 mV



NOTE: For best switching performance, the resistive load should be the same at the two differential outputs.

Figure 5. Resistive Load for V_{out} = 1 Vpp

Figure 5 shows the recommended method for supplying a full scale voltage of 1 V to the same 75 Ω load. The effective load on the MC44200 for the 1 V drive can be calculated as:

$$R_{LOAD} = 1\ V/20\ mA = 50\ \Omega.$$

The value for the parallel resistor necessary to achieve the 50 Ω load is:

$$1/Rp = 1/50 - 1/75 = 1/150.\ Rp = 150\ \Omega.$$

V_{DD} AND GND

To maximize the performance of the MC44200, noise should be kept to a minimum. Good printed circuit board design will enhance the operation of the MC44200. Separate analog and digital grounds will reduce noise and conversion errors. Sufficient decoupling and short leads will also improve performance (discussed later in this section).

When designing mixed analog/digital printed circuit boards, separate ground planes for digital ground and analog ground should be employed. Large switching currents generated by digital circuits will be amplified by analog circuitry and can quickly make a circuit unusable. Care should be taken to ensure analog ground does not inadvertently become part of the digital ground. The analog and digital grounds should be connected together at only one point. This is usually at or near where power enters the printed circuit board. Additionally, when interconnecting several printed circuit boards together, care must be taken to ensure that cabling does not interconnect digital switching currents through analog ground.

When using any device with the performance and speed of the MC44200, ground planes are essential. Loosely interconnected traces and/or random areas of ground strewn around the printed circuit board are inadequate for high performance circuitry. While distribution of V_{DDA} and V_{DDD} can be done by bussing, to do so with the ground system is disastrous.

A one inch long conductor is an 18 nH inductor. The cross sectional area of the conductor affects the exact value of the inductance, but for most PCB traces this is approximately correct. If the ground system is composed of traces or clumps of ground loosely interconnected, it will be inductive. The amount of inductance will be proportional to the length of the conductors making up the ground. This inductance cannot be decoupled away. It must be designed out.

A CMOS device exhibits a characteristic input capacitance of about 10 pF. If this gate is driven by a digital signal that switches 2.5 V in a period of 5 ns, the equation for the average current flowing during the switching time will be:

$$I_{AV} = Cdv/dt.$$

A voltage change of 2.5 V in 5 ns requires an average current of 5 mA. If we assume a linear ramp starting from zero, the total change in current will be 10 mA. The change in current per nanosecond per gate can be found by dividing the change in current by the time:

$$10\ mA/5\ ns = 2\ mA/ns.$$

For a device with 16 outputs driving one gate for each output:

$$di/dt = 16 \times 2\ mA/ns = 32\ mA/ns.$$

If the above 1–inch conductor is in this current path, then the voltage dropped across it can be found from the formula:

$$V = Ldi/dt = 18\ nH \times 32\ mA/ns = 0.576\ V.$$

If the inductor is in the ground system, it is in the signal path. The voltage generated by the switching currents through this inductor will be added to the signal. At best it will be superimposed on the analog signal as unwanted noise. At worst, it can render the entire circuit unusable. Even the digital signal path is not immune to this type of signal. It can false trigger clock circuits causing timing errors, confuse comparator type circuits, and cause digital signals to be misinterpreted as wrong values.

When laying out the PCB, use electrolytic capacitors of sufficient size at the power input to the printed circuit board. 47 µF tantalum capacitors are recommended. Adding low ESR (effective series resistance) decoupling capacitors of about 0.1 µF capacitance across V_{CC} and/or V_{DD} at each device will help reduce noise in general and ESD (electrostatic discharge) susceptibility. Connect the high–capacity and high–frequency capacitors as close as possible to all analog V_{CC}, digital V_{DD}, and ground pins. Implementation of a good ground plane ground system can all but eliminate the type of noise described above.

To summarize:

- Use sufficient electrolytic capacitor filtering
- Make separate ground planes for analog and digital ground
- Tie these grounds together at one and only one point
- Keep the ground planes as continuous and unbroken as possible
- Use low ESR capacitors of about 0.1 µF capacitance on 3 V_{CC} and V_{DD} at each device
- Keep all leads as short as possible

EMI

When using ICs in or near television receiver circuits, EMI (electromagnetic interference) and subsequent unwanted display artifacts and distortion are probable unless adequate EMI suppression is implemented. A common misconception is that some offending digital device is the culprit. This is erroneous in that an IC itself has insufficient surface area to produce sufficient radiation. The device, while it is the generator of interfering signals, must be coupled to an antenna before EMI is radiated. The source for the EMI is not the IC which generates the offending signals but rather the circuitry which is attached to the IC.

Potential EMI signals are generated by ***all*** digital devices. Whether they become a nuisance is dependent upon their frequency and whether they have a sufficient antenna. The frequency and number of these signals is affected by both circuit design within the IC and the manufacturing process. Device speed is also a major contributor of potential EMI. Because the design is determined by the anticipated application, the manufacturing process is fixed and the drive for speed ever increasing, the only effective point to implement EMI suppression is in the PC board design. The PC board usually is the antenna which radiates the EMI. The most efficient method of minimizing EMI radiation is to minimize the efficiency of this antenna.

The most common cause of inadequate EMI suppression lies with the ground system of the suspected digital devices. As pointed out previously, di/dt transitions can be significant in digital circuits. If the di/dt transitions appear in the ground system and the ground system is inductive, the harmonics present in these transitions are a source of potential EMI signals. The unfortunate result of putting digital devices on a reactive ground system is guaranteed EMI problems.

The area which should be addressed first as a potential EMI source is the ground. Without an adequate ground system, EMI cannot be effectively reduced by decoupling. If at all possible, the ground should be a complete unbroken plane. Figure 6 shows two examples of relieving ground around device pins. When relieving vias and plated through holes, large areas of ground loss should be avoided. When the relief pattern is equal to half the distance between pins, over etching and process errors may remove ground between pins. If sufficient ground around enough pins are removed, the ground system can become isolated or nearly isolated "patches" which will appear inductive. If ground, such as the vicinity of an IC, must be removed, replace with a cross hatch of ground lines with the mesh as small as possible.

If a single unbroken plane can be devoted to the ground system, EMI can usually be sufficiently suppressed by using ferrite beads on suspect EMI paths and decoupling with adequate values of capacitors. The value of the decoupling capacitor depends on the frequency and amplitude of the offending signals. Ferrite beads are available in a wide variety of shape, size and material to fit virtually any application.

Choose a ferrite bead for desired impedance at the desired frequency and construct a low pass filter using one or more appropriate capacitors in a "L", "T" or "PI" arrangement. Use only capacitors of low inductive and resistive properties such as ceramic or mica. Install filters in series with each IC pin suspected of contributing offending EMI signals and as close to the pin as possible. Analysis using a spectrum analyzer can help determine which pins are suspect.

Where PC board costs constrain the number of layers available, and if the EMI frequencies are far removed from the frequencies of operation, ferrite beads and decoupling capacitors may still be effective in reducing EMI emissions. Where only two (or in some cases, only one!) layer is used, the ground system is always reactive and poses an EMI problem. If the offending EMI and normal operating frequency differ sufficiently, filtering can still work.

While not generally recommended, in cases where a ground plane is not possible, the following technique may be used with some success.

An "island" is constructed in the ground system for the digital device using ferrite beads and decoupling capacitors as shown by the example in Figure 7. The ground must be cut so that the digital ground for the device is isolated from the rest of the ground system. Next choose a ferrite bead of the appropriate value. Install this bead between the isolated ground and the ground system. Install low pass filters in all suspect lines with the capacitor closest to the device pin connected to the isolated ground in all signal lines where EMI is suspect. Also cut the power to the device and insert a ferrite bead as shown in Figure 7. Finally, decouple the device between the power pin(s) and isolated ground pin(s) using a low inductive/resistive capacitor of adequate value.

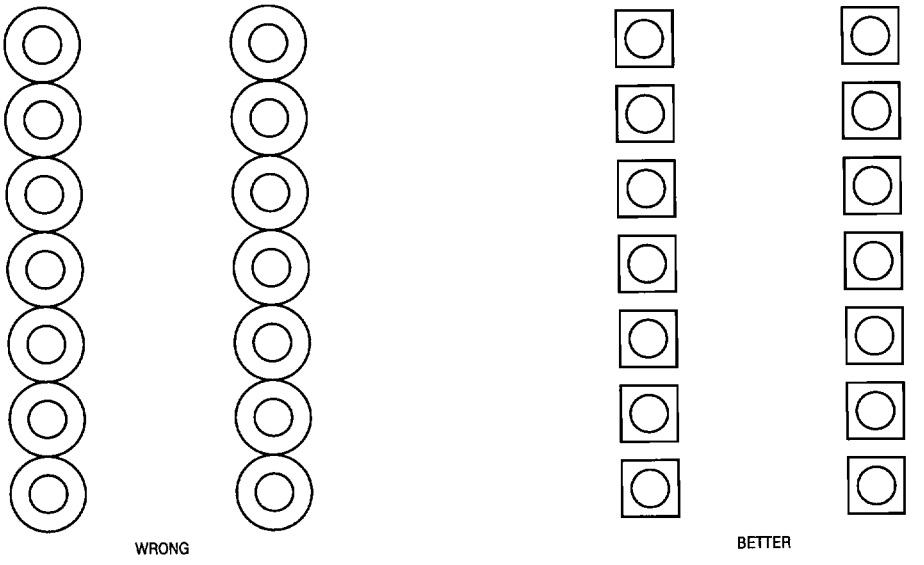


Figure 6.

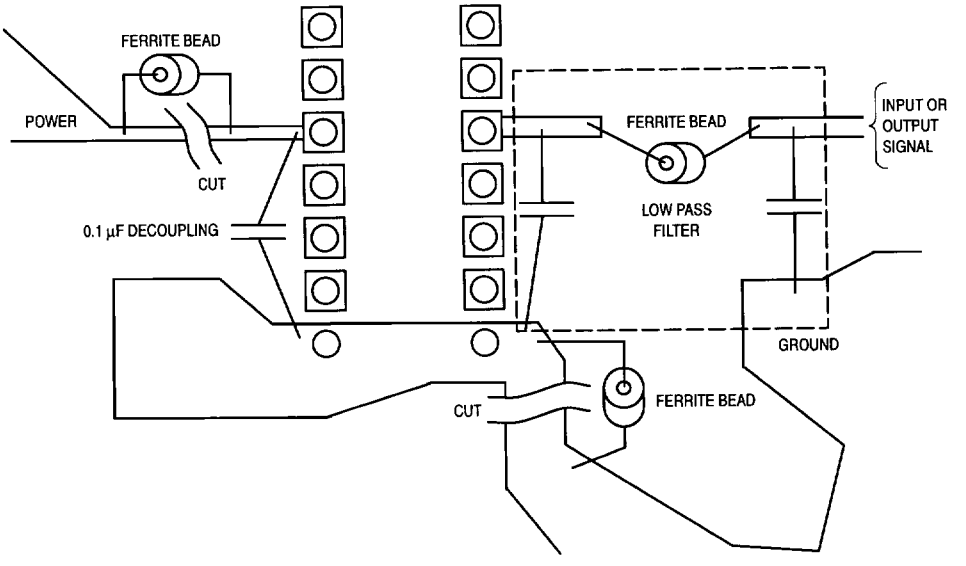


Figure 7.

The methods described above will work acceptably when the EMI frequency and the frequency of operation of the device generating the EMI differ greatly. Where the EMI is disturbing the high VHF or UHF channels and the device generating the EMI is operating within the NTSC/PAL bandwidth, the energy contained in the harmonics generating the EMI is situated well above the operating frequency and suppressing this type of EMI poses no great problem. However, if the EMI is present on low VHF channels and/or the operation of the device is outside the NTSC/PAL bandwidth, such as a 2x pixel clock or 4xfsc oscillator, compromise between video quality and suppression complexity is usually required to obtain an acceptable solution. For those cases where the operating frequency of the device is very near the frequency of the EMI disturbance, careful attention to PCB layout, multiple layer PCB and even shielding may be necessary to obtain an acceptable design.

LATCH–UP

The $V_{DD(A)}$, $V_{DD(D)}$, and $V_{DD(R)}$ pins connect to power supplies that are independent from each other. Therefore, latch–up may occur when the power is applied. To eliminate latch–up, apply power to the $V_{DD(A)}$, $V_{DD(D)}$, and $V_{DD(R)}$ pins simultaneously.

APPLICATION CIRCUIT

Figure 8 shows a typical application of the MC44200. The device has been biased for the low current (10 mA typical) mode. This drive allows the DAC to deliver 1.5 V into a doubly terminated, 75 Ω transmission line. The three bipolar transistors shown on the schematic provide the necessary current gain for the DAC outputs.

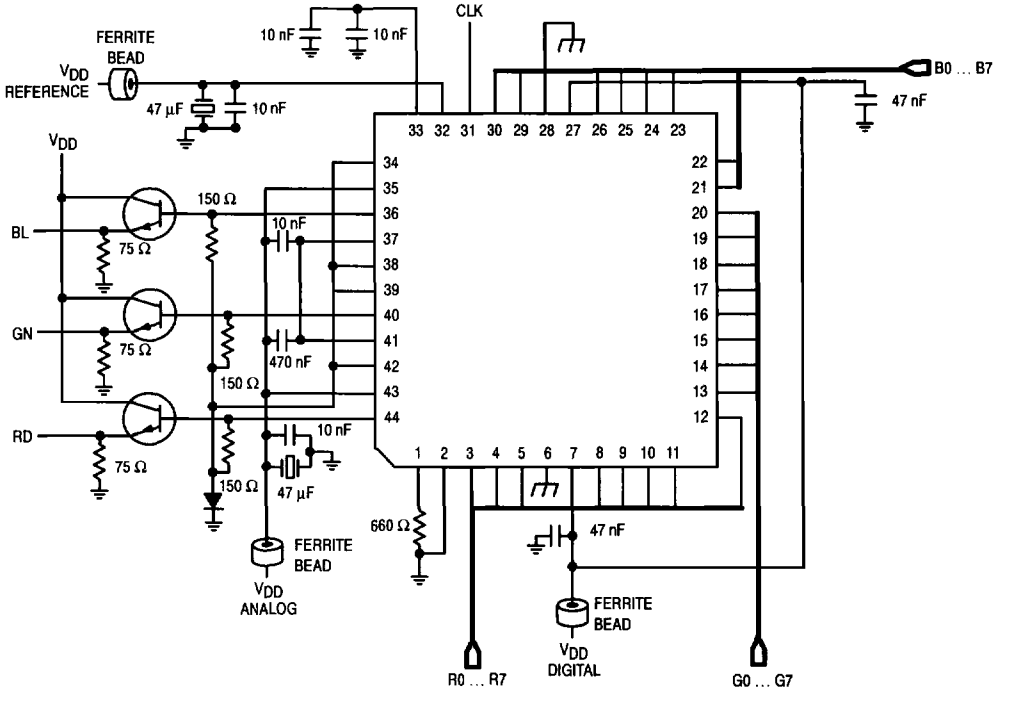
The 660 Ω resistor connected to I_{ref} (pin 1) sets the output drive:

$I_{out} = (V_{ref}/R_{ref}) \times K = (1.235\ V/660\ \Omega) \times 5.33 = 10\ mA.$

The voltage delivered to the load is:

$V_{out} = I_{out} \times R_{LOAD} = 10\ mA \times 150\ \Omega = 1.5\ V.$

If the diode shown in the schematic is chosen so that the forward voltage drop at 10 mA is equal to V_{BE} for the bipolar transistors, the base–emitter voltage drop of the transistors can be ignored.



NOTE: THE DEVICE IS IN LOW CURRENT MODE

ANALOG GROUND

DIGITAL GROUND

Figure 8. Triple Digital Analog Converter (Typical fixture for buffering)